Listing of Claims

1. (Currently Amended) A voltage regulation system for multiword programming in a non volatile memory, for example of the Flash type, with low circuit area occupation, wherein the memory comprises at least a memory cell matrix organized in cell rows and columns and with corresponding circuits responsible for addressing, decoding, reading, writing and erasing the memory cell content, each cell having a drain terminal connected to a matrix column and biased in the programming step with a predetermined voltage value by a program load circuit associated with each matrix column, the system further including, in parallel with each program load circuit, a current sinking conduction-to-ground path that includes an enabling ~~enabled by a~~ controlled active element.

2. (Original) The system according to claim 1, wherein the controlled active element is a pass transistor receiving on the control terminal thereof a first enabling signal.

3. (Original) The system according to claim 2, wherein the first enabling signal is complementary to a second enabling signal applied to the corresponding program load circuit.

4. (Original) The system according to claim 1, wherein the conduction-to-ground path is a redundant current path.

5. (Original) The system according to claim 1, wherein the conduction-to-ground path is a dummy current path.

6. (Currently Amended) A non-volatile memory circuit, comprising:

a non-volatile memory cell coupled to a bit line and a word line; and

a selectively actuated current sinking conduction to ground path coupled to the bit line.

7. (Original) The circuit of claim 6 wherein the non-volatile memory cell comprises a floating gate transistor having its drain terminal connected to the bit line and its gate connected to the word line.

8. (Original) The circuit of claim 6 further including a bit line biasing circuit coupled to the bit line, the selectively actuated conduction to ground path being connected in parallel with the bit line biasing circuit.

9. (Original) The circuit of claim 6 wherein the selectively actuated conduction to ground path is coupled to the bit line through at least a column decoding circuit.

10. (Original) The circuit of claim 6 wherein the selectively actuated conduction to ground path is coupled to the bit line through at least a bit line biasing circuit.

11. (Original) The circuit of claim 10 wherein the bit line biasing circuit and the selectively actuated conduction to ground path are oppositely activated.

12. (Original) A non-volatile memory, comprising:

a memory matrix including a plurality of memory cells arranged in columns, each associated with a bit line, and rows, each associated with a word line;

a column programming circuit coupled between a programming voltage source and each bit line and activated in response to a first control signal; and

a bypass path circuit for each bit line and coupled between the programming voltage source and ground and activated in response to a second control signal.

13. (Original) The memory of claim 12 wherein each memory cell comprises a floating gate transistor having its drain terminal connected to the bit line and its gate connected to the word line.

14. (Original) The memory of claim 12 wherein, for each column, the first and second control signals are complementary.

15. (Original) The memory of claim 12 further including a column decoding circuit for each column.

16. (Original) The memory of claim 12 wherein the bypass path circuit comprises a pass transistor for each column coupled between the programming voltage source and ground.

17. (Currently Amended) A voltage regulation system for a non volatile memory including a memory cell matrix organized in cell rows and columns, comprising:

a program load circuit for each matrix column that biases each memory cell in a selected matrix column with a predetermined voltage value during a programming operation; and

a current sinking conduction-to-ground path for each matrix column, each path being enabled when its associated matrix column is not selected during the programming operation.

18. (Original) The system of claim 17 wherein each memory cell comprises a floating gate transistor having its drain terminal connected to a bit line for a column and its gate connected to a word line for a row.

19. (Original) The system of claim 17 further including a column decoding circuit for each column.

20. (Original) The system according to claim 17, wherein the conduction to ground path includes a controlled active element comprising a pass transistor receiving on a control terminal thereof a first enabling signal.

21. (Original) The system according to claim 20, wherein the first enabling signal is complementary to a second enabling signal applied to the corresponding program load circuit.

22. (Original) The system according to claim 17, wherein the conduction-to-ground path is a redundant current path for the program load circuit.

23. (Original) The system according to claim 17, wherein the conduction-to-ground path is a dummy current path for the program load circuit.